GBIT/s PULSE REGENERATION AND AMPLIFICATION WITH GaAs-MESFETs

Heinz Beneking, Wilhelm Filensky
Institute of Semiconductor Electronics
Technical University Aachen
D-5100 Aachen, Templergraben 55
Federal Republic of Germany

Abstract

Using GaAs-MESFETs under switching conditions, the regeneration and amplification of fast pulses in the 50ps range is performed. Sharpening factors $\frac{t_{r_{in}}}{t_{r_{out}}}$ of 3 and voltage amplification factors of 2 at 50 ohm are reached for output pulses up to 100 mA.

Introduction

Modern communication systems use pulse code modulation. The proposed optoelectronic monomode glassfibre links will be able to transmit pulse rates of up to 5 Gbit/s. For these systems fast modulators as well as pulse regenerators and amplifiers are needed.

Because of its excellent switching behaviour, the GaAs-MESFET seems to be the favorable solution for pulse amplitude modulation (e.g. of the semiconductor laser[1,2]) as well as regeneration and amplification of electrical pulse trains.

In this paper it is demonstrated that pulse sharpening factors of the order of three $\left(\frac{t_{rise_{in}}}{t_{rise_{out}}};\ \frac{t_{fall_{in}}}{t_{fall_{out}}}\right)$ can be achieved (t_{rise}, $t_{fall} \approx$ 50ps). In a 50 ohm experimental setup a voltage amplification factor of 2 has been realized, this value depending on the design of the transistor and the line impedance.

Sharpening procedure

In this mode of operation the channel of the FET is pinched off using a negative gate-source voltage. The pulse to be sharpened and amplified must be large enough, to switch the FET from the off-to the on-state and vice versa ($V_{SS} \gtrsim$ 1,5 V at 50 ohm). In this way the drain current jumps from zero to the maximum value and vice versa. The turn on time needed to reach a drain current of a given value is determined by

- the input time constant including the voltage dependent input capacitance
- the gate-voltage-dependent transconductance
- the slope of the incoming pulse and
- the level of the incoming pulse.

The transit time in the intrinsic FET (~5ps) need not to be taken into account because it is much smaller than the above-mentioned effects.

As the output waveform is nearly independent of the drain source voltage, the pulse sharpening can be explained by the following effects:
The input pulse coming along the 50 ohm line to the gate first sees a nearly open loop and is reflected. Thus its amplitude will be doubled until clamping at the entrance port of the FET takes place. The clamping follows from the input gate capacitance, which increases abruptly as the gate voltage changes from negative to positive values. As this capacitance is in series with the 50 ohm ohmic source and other series resistances, the voltage change across it decreases as the gate input voltage becomes more positive due to its smaller reactance. Additionally at voltages larger than the threshold voltage the resistance of the input diode becomes smaller and smaller.

The simplified equivalent circuit of the FET is shown in fig. 1. For mathematical evaluation the voltage dependent C is assumed to comprise a junction diode connected in parallel to the gate-drain-Miller-capacitance. The capacitance then is given by

$$C = \frac{C_o}{\sqrt{1-\frac{v_c}{\phi}}} + C_{gd}\,(1+g_m R_L)$$

C_o : zero bias capacitance

ϕ : diffusion potential

$g_m R_L$: voltage amplification factor

Assuming a square relation between drain current and gate-source-voltage the static transconductance is

$$g_m = 2\left(1+\frac{v_c}{V_p}\right)\frac{I_s}{V_p}$$

I_s: saturation current at v_c = 0V

V_p: pinch-off voltage

The nonlinear differential equation, which governs the dependence of the intrinsic voltage $v_c(t)$ on the generator voltage in the case of a ramp function is:

$$v_g(t) = \frac{V_g}{t_o}t - V_B = v_c + RI_R\left(e^{\frac{v_c}{V_T}}-1\right) + \left\{\frac{4C_{gd}I_sR_LR}{V_p^2}v_c + RC_{gd}\left(1+\frac{2I_sR_L}{V_p}\right) + \frac{RC_o}{\sqrt{1-\frac{v_c}{\phi}}}\right\}\frac{dv_c}{dt}$$

$\frac{V_g}{t_o}$: slope of the ramp

V_B : bias voltage

I_R : leakage current of the diode

V_T : $\frac{KT}{q}$

Besides the effects of the entrance port the nonlinear voltage dependence of the transconductance, which suppresses the foot of the incoming pulse, is responsible for the pulse sharpening.

Fig. 2 illustrates the influence of transconductance and voltage dependent input capacitance (without clamping of the diode) for a 4-gate MESFET ($f_{max} \approx$ 20 GHz). The input amplitude is constant for all risetimes (1,5 V at 50 ohm) and just below the threshold voltage of the input diode. Beginning with the minimum large signal risetime of the MESFET itself ($\approx$100ps) σ increases till the maximum of σ = 1,9 at $t_{r_{in}}$ = 1,5 ns is reached. As the risetime of the input pulse increases further, the sharpening factor decreases, eventually caused by the time constant of deep-lying impurity centers with the electron trapping rate increasing with increasing electric field[3]. As the channel is widened by the input pulse, the electric field is reduced resulting in a smaller trapping rate and a larger drain-current. This effect becomes more and more pronounced at large risetimes of the input pulse and deteriorates the switching behaviour of the FET if no buffer layer is used.

Experimental results

The pulse sharpening effect is demonstrated in fig. 3 for different input amplitudes. From this figure the dependence of the output pulse time lag on the input pulse amplitude can be observed. If the transit time is defined at 50 % pulse hight, negative values occur due to the sharpening effect.

In fig. 4 the pulse sharpening and amplification of the 4-gate MESFET is demonstrated. A step recovery pulse generator with a t_r = 110ps risetime is used resulting in a risetime of t_r = 53ps at the output. The variation of the switching time as a function of the input amplitude can be clearly seen.

Fig. 5 demonstrates the pulse train regeneration for two different input amplitudes. Allowing for the possibility of cascaded sharpeners this figure indicates, that pulse rates of at least up to 3 Gbit/s should be attainable without any additional passive pulse forming network. To minimize resistive losses the MESFETs used in the experiments are four gate structures with a gate width of 800 μm and a gate length of 1 μm. The technology has been reported earlier[4].

Acknowledgment

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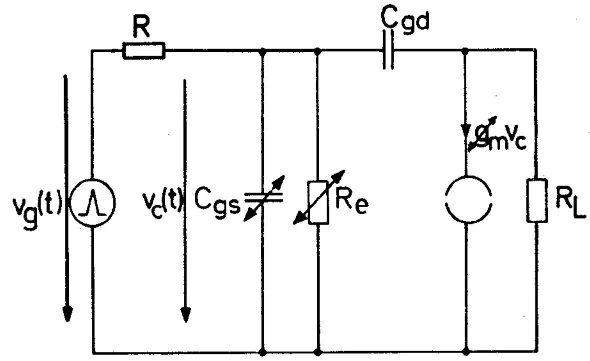

Fig. 1: Simplified equivalent circuit of the FET

R : internal gate resistance in series with the generator impedance

C_{gs}: gate-voltage dependent gate-source capacitance

R_e : gate-voltage dependent resistance of the input-diode

C_{gd}: gate-drain capacitance (assumed voltage-undependent)

g_m : gate-voltage dependent transconductance

R_L : load resistance

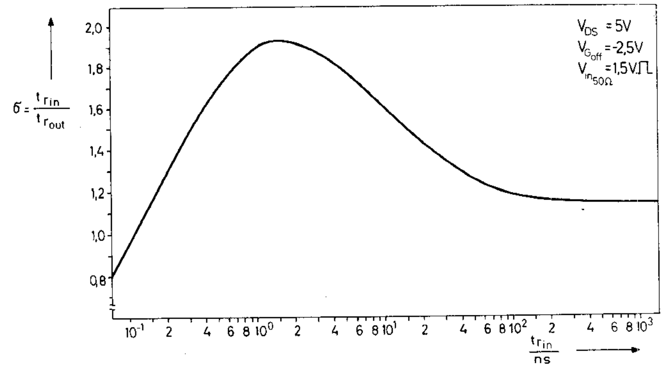

Fig. 2: Sharpening factor versus risetime of the input pulse

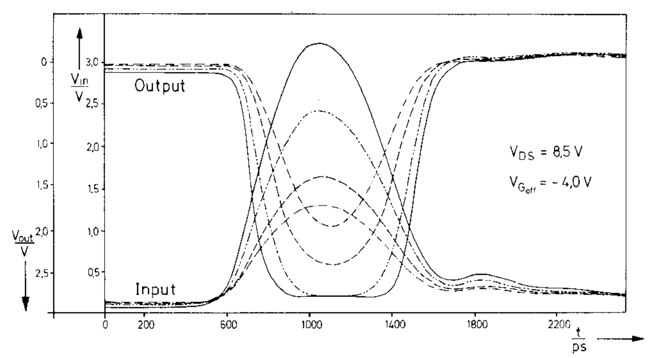

Fig. 3: Large signal behaviour MESFET driven by an avalanche generator. Load 50 ohm

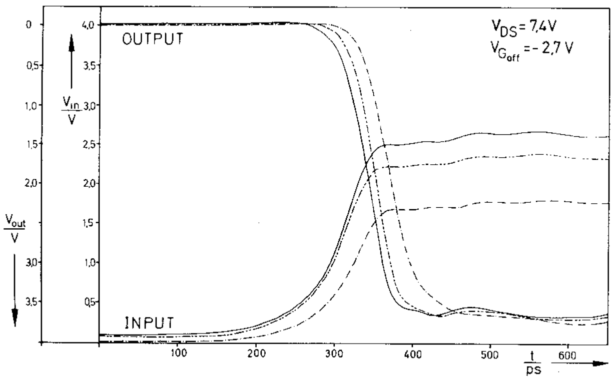

Fig. 4: Pulse sharpening and amplification. MESFET driven by a step-recovery pulse generator.

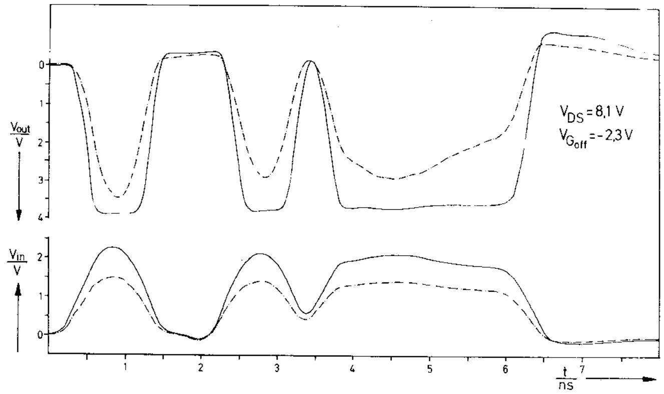

Fig. 5: Pulse train sharpening and amplification. Load 50 ohm, switching power 0,3 W, MESFET driven by an avalanche word generator.